Code.No: 43216 | R07 | SET-4

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
II.B.TECH - I SEMESTER REGULAR EXAMINATIONS NOVEMBER, 2009
DIGITAL LOGIC DESIGN
(Common to CSE, IT, CSS)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1. a) Express the Excess-3 code as a Gray cods
   b) What is meant by Self complementing codes? Give an example and explain.
   c) What are the properties of Boolean algebra? [8+8]

2. a) State and prove De'Morgans theorems
   b) Prove that NAND and NOR gates are universal gates
   c) Design a 2 input XOR and XNOR using NAND and NOR gates respectively by using only 4 gates each. [16]

3. a) Design a FULL adder / subtractor unit using only NAND gates
   b) Minimize the given function f = $\sum(1,2,3,5,7,9,11,13)$ use K map method. [8+8]

4. a) Design a Priority encoder of 4 bit.
   b) Write HDL code to model the above encoder. [8+8]

5. a) Design a finite state machine which can detect the sequence 0010 by using JK flip flops. [8+8]
   b) Write HDL program in Behavioral model to design the above sequence detectors.

6. a) Design an asynchronous modulo-6 counter. Use SR flip flop in the design.
   b) Write HDL program to model in structural model. [8+8]

7. a) Design a 4 bit number square generated using ROM.
   b) Write a brief note on sequential programmable devices. [8+8]

8. Write brief note on
   a) Static and dynamic hazards.
   b) Flow table generation in asynchronous limits in pulse mode. [8+8]

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